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flip-flop + input + random delay

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The basic D **flip-flop** is a sequential device that transfers the value of the d **input** to the q **output** on every rising edge of the clock clk ...

myhdl.jandecaluwé.com/doku.php/cookbook:ff - 32k - Cached - Similar pages

9-5-4: ALS Gates

The Linear timing distribution is used to specify a **random delay** period that ... For example, the set and reset inputs of a **flip flop** should be tied low if ...

www.staticfreesoft.com/jmanual/mchap09-05-04.html - 17k - Cached - Similar pages

(WO/2001/067231) METHOD AND APPARATUS FOR GENERATING RANDOM ...

A **flip-flop** is clocked with an **input** that deliberately violates the setup or hold ... utilizes the time **delay** between mistakes to generate a **random** number. ...

www.wipo.org/ipd/IPDL-CIMAGES/view/pct/getbykey5?KEY=01/67231.020103 - 36k - Cached - Similar pages

Information signal **delay system utilizing **random** access memory ...**

The VCLK signal is directly applied to one **input** terminal of an exclusive-OR gate 52 and is delayed in an RC **delay** circuit 54 and presented to another ...

www.freepatentsonline.com/4633331.html - 41k - Cached - Similar pages

Digital randomizer for on-chip generation and storage of **random ...**

a plurality of N1 D-type flip-flops, each **flip-flop** including: a **clock input** port coupled to a common jitter clock signal; a **delay input** port coupled to ...

www.freepatentsonline.com/5570307.html - 54k - Cached - Similar pages

High-Speed Random-Data Generator Facilitates Eye Diagrams - Maxim ...

The choice of amplifier, comparator, and **flip-flop** depends on the ... amount of **random** data, the comparator's propagation **delay** should be comparable to the ...

www.maxim-ic.com/appnotes.cfm/appnote_number/3471 - 23k - Cached - Similar pages

[PDF] Part I: Designing Basic Processor Elements 1-input INV: area: 4 ...

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What is the **area/delay** product? d. Design a 2-bit adder using any **random** logic. ... Next you need to create aD **flip flop** using D-latches and any other ...

www.ece.ucsb.edu/~kastner/ece154/homework/HW2.pdf - Similar pages

[PDF] A DYNAMIC LOGIC CIRCUIT EMBEDDED FLIP-FLOP FOR ASIC DESIGN

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than conventional master-slave **Delay flip-flop**, but ... For power estimation, we used two **input** patterns: complete **random** patterns and probabilistic ...

www.ap-asic.org/2000/proceedings/2-1.pdf - Similar pages

Circuit forms **random-bit-sequence generator - 5/10/2001 - EDN**

Ideally, this **flip-flop** should provide a **rand** m bit sequence. Unfortunately, when the data at the **flip-flop's input** changes simultaneously with the clock's ...

www.edn.com/article/CA82766.html?1=1 - Similar pages

[PDF] Duty Cycle Measurement and Correction Using a **Random Sampling ...**

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[EETimes.com - Clock domain modeling is essential in high density ...](#)

All **clock domain crossing** logic should be contained in the bus adapter module. ...

verification tool that accurately handle **asynchronous clock** domains and ...

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All **clock domain crossing** logic should be contained in the bus adapter module. ...

synchronized by introducing a synchronization **flip-flop** with no logic in ...

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complex SoC environment for designers to verify **clock domain crossing** and system ...

that correctly model **asynchronous** behavior in **multi-clock** designs. The ...

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Multiple Pseudo Asynchronous clocks - phase shifted synchronous **clocks** with ...

Careful analysis of metastability in the **cross-domain** re-synchronization ...

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tool to reproduce synchronization bugs by introducing **random one-clock jitter** in **cross domain** signals [5, 6]. A fundamental difference between our work and ...

[www.cs.indiana.edu/~lepike/pubs/dcc.pdf](#) - Similar pages

[\[PDF\] A MULTIPLE-CLOCK-DOMAIN BUS ARCHITECTURE](#)

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For the purposes of this dissertation, **cross-talk** can be important since ... **clock cycle delay** within **clock domain 1** since the **flip flop** on the left and the ...

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Multiple asynchronous clock domain. signals converging on <gate name> ... **crossing clock domain** should be Gray coded." Whenever a multi-bit signal ...

[www.synopsys.com/news/pubs/verib/q404/va_vcl4_iss3.pdf](#) - Similar pages

[Using delay - Patent Storm](#)

A method for distributing **clocks** to **flip-flop** circuits which constitute a logic ... the virtual **delay element** is coupled to an **asynchronous us** circuit element. ...

[www.patentstorm.us/class/713/401-Using_delay.html](#) - 47k - Cached - Similar pages

[12.4 An overview of DE demos](#)

12-19 shows some simple demonstrations of **multiple domain** simulations. ... The **asynchronous** events are plotted together with a **clock**, which produces ...



(verify OR verification) cycle (metastable OR ... Search

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Using Assertion-Based Verification to Verify Clock Domain

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Crossing Signals - group of 2 »

C Kwok, VV Gupta, T Ly - DVCon, February, 2003 - 0-in.com

... USING ASSERTION-BASED VERIFICATION TO VERIFY CLOCK DOMAIN ... one bit will change in a given **cycle** (eg, Gray ... Design & Verification Conference (DVCon) Technical Paper ...

Cited by 3 - View as HTML - Web Search

Fourteen ways to fool your synchronizer - group of 7 »

R Ginosar - Asynchronous Circuits and Systems, 2003. Proceedings. Ninth ... , 2003 - ieeexplore.ieee.org

... A powerful protocol **verification** algorithm might provide a useful ... The added **cycle** time provides an extra safety factor ... should be carried out to **verify** that all ...

Cited by 18 - Web Search

CLOCK DOMAIN CROSSING - group of 2 »

R Biddappa - cadence.co.in

... techniques can be used to **verify** the stability ... clock domain synchronization – Functional **verification** for data ... clock-related iterations in the design **cycle** ...

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Cycle error correction in asynchronous clock modeling for cycle-based simulation - group of 2

»

J Lee, J Yi - Proceedings of the 2006 conference on Asia South Pacific ... , 2006 - portal.acm.org

... C simulation outputs as a testbench for RTL **verification**. ... propose a technique to correct the **cycle** errors ... clock domains, there exists a **metastability** problem [8 ...

Web Search

Asynchronous interconnect for synchronous SoC design - group of 4 »

A Lines, F Microsystems - Micro, IEEE, 2004 - ieeexplore.ieee.org

... has no timing assumptions to **verify** and operates ... we developed and applied many **verification** and test ... for a larger portion of their **cycle** than synchronous ...

Cited by 8 - Web Search - BL Direct

Formal Verification of Synchronizers - group of 5 »

T Kapschitz, R Ginosar - Lecture notes in computer science - www-ee.technion.ac.il

... Formal **Verification** of Synchronizers 7 **cycle**, but meanwhile R1 may reach the receiver (recall T ... It is insufficient to **verify** that data is loaded into the sender ...

Cited by 3 - View as HTML - Web Search

Asynchronous Interconnect for Synchronous SoC Design

AI PIPELINING - doi.ieeecomputersociety.org

... design has no timing assumptions to **verify** and operates ... we developed and applied many **verification** and test ... a larger portion of their **cycle** than synchronous ...

Web Search

Nexus: an asynchronous crossbar interconnect for synchronous system-on-chip designs

A Lines - High Performance Interconnects, 2003. Proceedings. 11th ... , 2003 - ieeexplore.ieee.org

... It has no timing assumptions to **verify**, and operates ... This is done with a **m** **tastable** circuit using **cross** ... the result determines whether the next **cycle** advances or ...



circuit verification + (multi OR multiple) clock +

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Automatic verification of asynchronous circuits - group of 2 »

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TWS Lee, MR Greenstreet, CJ Seger - Design & Test of Computers, IEEE, 1995 - ieeexplore.ieee.org

... make it easy to show that the **circuit** in Figure ... Transitions for the design and **verification** of self ... Transitions specify state changes using **multi-** assignments. ...

Cited by 13 - Web Search - BL Direct

Simulation based verification of register-transfer level behavioral synthesis tools - group of 2 »

»

R Ernst, S Sutarwala, JY Jou, M Tong - Design Automation Conference, 1990 EDAC. Proceedings of the ..., 1990 - ieeexplore.ieee.org

... is resynthesized by a **multi-level logic** ... **System Verification Function** The **verification** system configuration is ... back to "0", the normal **circuit** operation is ...

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Using Assertion-Based Verification to Verify Clock Domain Crossing Signals - group of 2 »

C Kwok, VV Gupta, T Ly - DVCon, February, 2003 - o-in.com

... synchronizer is a **circuit** that conditions ... Design & Verification Conference (DVCon)

Technical ... Techniques for Designing Multi- Asynchronous Clock Designs," SNUG ...

Cited by 3 - View as HTML, - Web Search

Performance of synchronous and asynchronous schemes for VLSI systems - group of 6 »

M Afghahi, C Svensson - IEEE Transactions on Computers, 1992 - doi.ieeecs.org

... resembles a conventional clocked sequential **circuit**, namely, globally ... models for synchronous and **asynchronous** schemes are ... variation of a single **clock** path and ...

Cited by 55 - Web Search

Advanced synchronous scan test methodology for multi clock domain ASICs - group of 2 »

J Schmid, J Knablein - VLSI Test Symposium, 1999. Proceedings. 17th IEEE, 1999 - ieeexplore.ieee.org

... DFT insertion, test program generation and **verification** must also ... named STMCs (Scan Technique for Multi Clock Systems) [4 ... By means of this the **circuit** is made ...

Cited by 7 - Web Search

A Distributed Approach to Timing Verification of Synchronous and Asynchronous Digital

Designs - group of 3 »

S Ghosh - Computer-Aided Design of Integrated Circuits and Systems, ..., 1987 - ieeexplore.ieee.org

... digital design is one wherein a single **clock** or **multiple clocks** that are ... and a **random** pulse generator and then explains **verification** of the **circuit** in the ...

Web Search

On path delay testing in a standard scan environment - group of 3 »

P Varma, CCT Inc, CA San Jose - Test Conference, 1994. Proceedings., International - ieeexplore.ieee.org

... that cause an increase in the delays of **circuit** paths, has ... **clock** suppression techniques to take advantage of **clock** gating or **multiple clocks** in the ...

Cited by 17 - Web Search - BL Direct

CAD Tools and Algorithms of Processor-based Logic Emulators

AA Yazdanshenas - vlsi.uwindsor.ca